Jukka Väyrynen
Antti H. Rauhala
Simo Murtojärvi

DUAL MODE MULTI-SLOT EGPRS TRANSMITTER

DUAL MODE MULTI-SLOT EGPRS TRANSMITTER

TECHNICAL FIELD:

This invention relates generally to radio frequency (RF) transmitters and, more specifically, relates to dual mode RF transmitters, such as those found in wireless voice and/or data telecommunications terminals, such as cellular telephones.

BACKGROUND:

In one existing type of General Packet Radio System (GPRS), that uses only Gaussian Mean Shift Keying (GMSK) modulation, the transmitted power of a dual timeslot transmitter is changed directly from the power level of the first timeslot to the level of the second timeslot (i.e., there is no power ramping between adjacent timeslots).

However, in at least one proposed dual timeslot system known as Enhanced General Packet Radio Service (EGPRS), both GMSK and 8-PSK modulation is used, and the modulation sequence is changed from GMSK to 8-PSK, or vice versa, during the transition period. However, this approach would thus require that both timeslots are driven in the EDGE (Enhanced Data rate for Global Evolution) Mode, characterized by having fixed power amplifier (PA) gain power control, if at least one of the transmitted timeslots contains 8-PSK modulation. If only GMSK modulation is used in both timeslots, the transmitter would operate in the GMSK mode with a variable gain PA.

This approach would also set Iref according to the timeslot having the higher power level, and would drive the PA during both timeslots with a common value of Iref (Iref sets the PA quiescent current in the EDGE mode).

The inventors have realized that several problems can be experienced using the approach outlined above. A first problem relates to the available PA output power with the PA operated in the EDGE Mode with GMSK modulation. The GMSK power in the EDGE Mode is currently not defined in the PA specifications, and to operate the PA in the EDGE mode, with both GMSK and 8PSK modulation, would almost double the number

of PA parameters that would need to be specified. With current commercially available PAs, that operate in the 850/900 MHz band, the power class drop to +29 dBm is a requirement, but to achieve this the transmit (TX) gain digital attenuator would need to be set to almost its minimum value to obtain the specification requirement of +26.5 dBm output power, in extreme conditions, with a safe margin. This TX gain attenuator setting difference also results in an additional tuning operation during manufacturing. In the 1800/1900 MHz band there is also a problem achieving +30 dBm power class (tolerance +/2, +/-2.5 in extremes), even with minimum TX gain attenuation. This may imply that the only possible solution in the 1800/1900 MHz band (GMSK) to reduce power is a class drop to +24 dBm.

A second problem relates to the production tuning operations, as they would be made more complicated if the same Iref value is used for both timeslots. For example, with the maximum Iref value all TX power levels need to be tuned, with the middle Iref value two thirds of the power levels would have to be re- tuned, and one third of the power levels would be required to be tuned three times. In addition, all of the required tuning tables would need to be saved in the software of the mobile station.

A third problem relates to avoiding discontinuities in the TX Inphase and Quadrature phase (I/Q) signals to ensure a smooth power transition between the 8-PSK and GMSK (and vice versa) time slots.

A fourth problem arises from the use of the same value of Iref for both timeslots, as this causes poor efficiency in the timeslot having the lower TX power level.

A fifth problem arises from the power detector sensitivity of the at least some commercially available PAs. The PA power detector in essence loses sensitivity with a maximum Iref at +19 dBm, which means that the operation of the power control loop is impaired with power levels below that value.

SUMMARY OF THE PREFERRED EMBODIMENTS

The foregoing and other problems are overcome, and other advantages are realized, in accordance with the presently preferred embodiments of these teachings.

In accordance with a presently preferred dual mode EGPRS transmitter system embodiment, all RF controls are changed between adjacent TX timeslots according to the modulation type of the next timeslot, including the transmitter mode. As a result, optimized controls for each of GMSK (variable gain PA) and 8-PSK (fixed gain PA) single slot operation can be used in the multi-slot operation, without compromising RF performance. This includes full GMSK/EDGE power, and optimum efficiency for both independent timeslots. Output power ramping is employed between two adjacent timeslots.

In accordance with the presently preferred dual mode EGPRS transmitter embodiment, all of the RF controls that would be used in a single timeslot GMSK, and in a single timeslot 8-PSK transmitter, are used in the multi-slot transmission mode. The RF settings are changed during a guard period between adjacent timeslots. For example, the PA operating mode includes the bias voltages, the power control method (fixed gain PA to variable gain PA), and the characteristics of the power control loop are changed during the guard period so as to be appropriate for the modulation type of the next timeslot.

In this presently preferred dual mode solution, there are no compromises made during multi-slot operation. That is,. the RF performance of independent time slots is equivalent to that which can be achieved when operating with a fully optimized single timeslot.

In addition, the production tuning procedures used with a conventional single timeslot transmitter can be used in the multi-slot case, thereby eliminating the complexity and additional expense of performing additional multi-slot tuning procedures during production.

In the presently preferred dual mode multi-slot operation the TX power is ramped

between adjacent timeslots to avoid power transients when switching the PA mode, the power control loop, and so forth, during the transition period.

A method is disclosed to operate a dual mode multi-timeslot RF transmitter, as is an RF transmitter that includes a control unit that operates in accordance with the method. The method includes, prior to a first timeslot, setting a plurality of control signals for the RF transmitter in accordance with a first modulation format used during the first timeslot; and during a guard period between the first timeslot and a next, temporally adjacent timeslot, setting the plurality of control signals for the RF transmitter in accordance with a second modulation format used during the second timeslot, where the first modulation format differs from the second modulation format.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other aspects of these teachings are made more evident in the following Detailed Description of the Preferred Embodiments, when read in conjunction with the attached Drawing Figures, wherein:

Figs. 1A and 1B, collectively referred to as Fig. 1, show a simplified block diagram of a multi-slot transmitter in accordance with this invention, where Fig. 1A shows the configuration of the multi-slot transmitter in the GMSK case with a variable gain PA, and Fig. 1B shows the configuration of the multi-slot transmitter in the 8PSK case with a fixed gain PA;

Fig. 2 is a basic timing diagram that illustrates the multi-slot operation of the multi-slot transmitter of Fig. 1;

Fig. 3 is a more detailed timing diagram that shows the transition of a plurality of RF control signals when going from a GMSK timeslot to an 8-PSK timeslot; and

Fig. 4 shows the transition of the plurality of RF control signals when going from an 8-PSK timeslot to a GMSK timeslot.

4

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a simplified block diagram of a multi-slot transmitter (MST) 10 in accordance with this invention, where Fig. 1A shows the configuration of the multi-slot transmitter in the GMSK slot case with a variable gain PA 12, and Fig. 1B shows the configuration of the multi-slot transmitter in the 8PSK slot case with the PA 12 operated in the fixed gain mode. An output power detector 14 provides a power detection signal (DET) 14A to an RF block, here implemented for convenience in an RF ASIC 16. The DET signal 14A is applied to one input of an error amplifier 18. The RF ASIC 16 also includes an I/Q modulator portion implemented as a direct conversion mixer 20 having an output that is fed to a digital RF attenuator (TX_gain) 22. The output of TX_gain 22 is input to an ALC RF attenuator 24 that, in the embodiment of Fig. 1A, is operated as a fixed gain buffer amplifier, and in the embodiment of Fig. 1B is operated as a variable RF attenuator controlled by an ALC signal 18A that is output from the error amplifier 18, and selectively applied through a switch 26. In the embodiment of Fig. 1A the error amplifier output signal 18A is referred to as Vcntrl or Vpc (shown in Figs. 2, 3 and 4), and is applied to the PA 12 for controlling its gain. Input signals include a Mode signal 1 (shown as Vmode in Figs. 3 and 4), the I and Q input signals to be transmitted (TXI 2 and TXQ 3), TXP 4 and TXC 5 that are applied to the error amplifier 18 (both shown in Figs. 3 and 4), and for the case of the fixed gain PA 12 embodiment of Fig. 1B, an IREF signal 6 and a TXA signal 7 (both shown in Figs. 3 and 4). TXA 7 controls the state of the switch 26 and during the power ramping period in the 8-PSK mode is asserted low (see Figs. 3 and 4) to close switch 26, thereby applying the output of the error amplifier 18 to the control input of the ALC RF attenuator 24. During the active portion of the 8-PSK timeslot, TXA 7 is driven high to open switch 26, thereby avoiding amplitude cancellation caused by the closed power control loop. TXP 4 is an enabling signal for the error amplifier 18, and in Fig. 3 can be seen to be active during both the GMSK and 8-PSK slots, and to be deasserted (low) during the guard time between slots. The mode signal 1, when low, places the PA 12 into the variable gain mode of operation, and when high places PA 12 into the fixed gain mode of operation (where IREF sets the PA 12 quiescent current). The TXC (transmit control) signal 5 is varied to control the output power level, either via the Vpc signal 18A in the variable gain PA 12 mode of Fig. 1A,

or via the ALC control applied to the ALC RF attenuator 24 in the fixed gain PA 12 mode of Fig. 1B. The TXC signal is ramped during the guard time between the GMSK and 8-PSK slots, as can be seen in Figs. 3 and 4.

Preferably all RF control signals settings are changed during the guard period between adjacent timeslots. This changes the PA 12 operating Mode, including bias voltages, the power control method (from fixed gain PA 12 to variable gain PA 12), and the power control loop from DET 14 to the error amplifier 18, and from the error amplifier 18 to either the PA 12 or the ALC RF attenuator 24, via the Vpc or the ALC control signal, respectively. Changing the PA Mode 1 between timeslots ensures full power operation for the GMSK timeslot.

In the embodiment shown in Figs. 1B and Fig. 2 the TXA 7 and Iref 6 signals are used only for the EDGE timeslot (only for the 8-PSK modulation case), and both Iref 6 and Mode 1 are changed between timeslots. In addition, the Vpc signal is used for GMSK modulation and the ALC control signal is used for 8-PSK modulation.

Note that in Figs. 3 and 4 the TX I/Q may be made a constant sine wave during the Iref (and Mode) change, to avoid power spikes that would result in a spreading of the output spectrum. However, this is not necessary, as the output power is ramped down before switching Iref 6 and Mode 1.

At the points labeled 1 and 2 in Fig. 2, the falling ramp of the first time slot (GMSK or 8-PSK) is ramped down to the base level. At Point 1 the Mode 1 and Iref 6 signals are set according to the requirements of the next timeslot, and the base level of the next timeslot is written (TXC, shown in Figs. 3 and 4).The base level voltage is assumed to have sufficient time to settle before Point 2. As a result, all dual-slot rising and falling power ramps (GMSK and 8-PSK) operate in a manner that is similar to the conventional single timeslot case.

In the preferred embodiment the time between two adjacent timeslots is 34.13 microseconds (corresponding to 9.25 symbols, tail bits not included). For the timing

between two timeslots the TXC ramp up/down time is about 12 microseconds, and the time between Points 1 and 2 in Fig. 2 is about 10 microseconds.

Referring also to Fig. 3, preparation for the first timeslot is performed as in the conventional single timeslot case. That is, TXC 5 is raised first to the base level, followed TXC 5 ramp up. The RF controls are thereafter operated similar to the single timeslot case until the falling ramp of the first timeslot. The falling ramp of the first timeslot (the GMSK slot in this example) is ramped down to it's base level. At this time the PA Mode 1 is changed to EDGE, TXP 4 is deasserted (goes low), and the base level of the next timeslot is written (TXC). Note that in Fig. 1B (8-PSK operation) Vpc is set to 2.8V (if needed by the PA 12), and the ALC voltage controls the power level.

There are three commands issued to the RF ASIC 16 (such as over an RF ASIC serial bus interface, not shown) during the guard period. These commands are used for controlling Vpc, changing the power control loop, shutting down the buffer mode and setting the proper TX gain with the digital attenuator 24. In addition, Vpc is set to 2.8V in the EDGE mode. After these commands are issued during the guard period, TXP 4 is raised, Iref 6 is adjusted according to the needs of the next timeslot and the rise in the TXC ramp for the next timeslot is started.

At the end of second timeslot, Iref is set to some value, such as 5 mA, to ensure PA 12 stability after an antenna switch opens (controlled by Vant). After the antenna switch control signal opens the antenna switch, other PA 12 control voltages (VTXP, Vpc) are turned off.

Referring to Fig. 4, as in the case of Fig. 3 the preparation for first timeslot can be performed as in the conventional single timeslot case. Iref 6 is raised to some predetermined value, such as 5 mA, before the Vant control signal is asserted to ensure PA 12 stability. TXC 5 is then raised first to the base level, followed by TXC ramp up. The control signal operation is then similar to the single EDGE (8-PSK) timeslot case until the falling ramp of the first timeslot. The falling ramp of the first time slot is ramped down to the base level, the PA 12 Mode is changed to GMSK, TXP 4 is

deasserted, and the base level of the next timeslot is written (TXC 5). During the guard period Iref 6 is set to the predetermined level (e.g., 5mA) for a short while to avoid spikes in RF power. TXP 4 is then raised and TXC 5 is ramped up for the next timeslot to be started.

5   As is shown in Figs. 1A and 1B, a control unit 100 is provided for changing the states of the various control signals as discussed above and shown in Figs. 2, 3 and 4. The control unit 100 may be implemented with state machine logic, with a programmed microcontrol unit, or by any suitable means.

It should be noted that the control logic can differ between PAs 12 provided by different
10   suppliers. For example, one conventional PA does not require 2.8V Vpc voltage in the EDGE mode, and the Iref logic has the opposite sense to that shown in the drawings. Thus, the specific signal levels and transitions shown in Figs. 3 and 4 are exemplary, as those skilled in the art will recognize that modifications may need to be made depending on the type of PA 12 that is selected for use in a given application. Further, this invention
15   is not limited for use only with 8-PSK and GMSK modulation formats, and furthermore is not to be considered to be limited by the specific timing relationships, timing values and signal levels depicted in Figs. 3 and 4.

Thus, while this invention has been shown and described in the context of certain presently preferred embodiments thereof, it is expected that those skilled in the art may
20   derive various modification to these embodiments when guided by the foregoing description of the invention. However, all such modifications will still fall within the scope of this invention.